corresponding substrate surfaces. This method includes defining spatial characteristics for each of the spiral conductive patterns; determining the number of spiral conductive patterns; calculating the number of turns for each of the spiral conductive patterns; and selecting a spiral shape for each of the spiral conductive patterns.

[0017] The present invention advantageously enables the replacement of costly discrete inductors with less expensive printed inductors. This replacement may occur without an increase in inductor footprint sizes.

BRIEF DESCRIPTION OF THE FIGURES

[0018] The present invention will be described with reference to the accompanying drawings. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the reference number.

[0019] FIGs. 1A and 1B are views of printed inductor patterns;

[0020] FIG. 2 is a view of a substrate attached to an aluminum housing;

[0021] FIG. 3 is a view of an exemplary multiple layer substrate;

[0022] FIG. 4 is a view of a meander line inductor;

[0023] FIG. 5 is an illustration of a multiple layer inductor;

[0024] FIGs. 6A and 6B are views of a three layer spiral inductor implementation;

[0025] FIGs. 7 an 8 are views of a five layer spiral inductor implementation;

[0026] FIGs. 9A and 9B are views of an exemplary round spiral shape;

[0027] FIGs. 10A and 10B are views of an exemplary square spiral shape;

[0028] FIGs. 11A and 11B are views of an exemplary hexagonal spiral shape;

[0029] FIGs. 12A and 12B are views of an exemplary octagonal spiral shape;

[0030] FIGs. 13 and 14 are views of exemplary side shield patterns;

[0031] FIG. 15 is a flowchart of an inductor design procedure;

[0032] FIG. 16 is a block diagram of an exemplary communications node;

[0033] FIG. 17 is a circuit schematic illustrating implementations of upstream and downstream filters; and

[0034] FIGs. 18A and 18B are views of a printed diplexer.

DETAILED DESCRIPTION OF THE INVENTION

I. Introduction

[0035] Electronic products are typically implemented on substrates, such as PCBs, that have one or more layers. Each of these layers includes a non-conductive surface upon which electronic components and traces (also referred to herein as conductive routing) may be disposed. Traces are patterns of conductive material, such as copper, disposed on a non-conductive substrate surface that provide electrical interconnections between electronic components. In addition to providing interconnectivity, traces may provide electromagnetic shielding to electronic components and their interconnections.

[0036] A substrate may support various types of electronic components. Two such component types are printed components and discrete components. Printed components are created through the integration of a material with one or more substrate surfaces in a specified pattern. An exemplary printed component material includes conductors for the creation of components such as resistors, capacitors, and inductors. Further exemplary materials include dielectrics for the creation of components such as capacitors and transmission lines.

[0037] Printed components may be placed on a substrate surface through various techniques. In one such technique, a substrate surface is first covered with a material layer, such as a conductive metal. Next, through chemical reduction processes and or mechanical routing, undesired portions of this material layer are etched away. This etching results in one or more printed electronic components

being disposed on the substrate surface. In other printing techniques, components are formed through the use of materials, such as conductive inks and solder flux.

[0038] In contrast to printed components, which are created through an integration process with one or more substrate surfaces, the assembly of discrete components does not require a substrate. Examples of discrete components include leaded components, surface mounted components, and integrated circuits (ICs). Discrete components have terminals that attach to metal traces on a substrate. The attachment of these terminals is performed through techniques, such as soldering.

[0039] As described above, many substrates include a plurality of surfaces. These surfaces may be arranged in a layered pattern. FIG. 3 is a side view of an exemplary multiple layer substrate 300 having surfaces 302a through 302f. In such multi-layer arrangements, pairings of adjacent surfaces (e.g., surfaces 302b and 302c) are each separated by a non-conductive material(s) 304, such as epoxy-glass composite. Multi-layer substrates have outer surface layers and one or more inner surface layers. Outer surface layers are adjacent to only one other surface layer. The exemplary substrate of FIG. 3 includes outer layers 302a and 302f. In contrast, for each inner surface layer, there are two adjacent surface layers. The exemplary substrate of FIG. 3 includes inner layers 302b, 302c, 302d, and 302e.

[0040] Multi-layer substrates, such as the exemplary substrate shown in FIG. 3, may provide for the interconnection of components supported by different layers. Such interconnections are supported by vias. Vias are apertures that penetrate one or more substrate surfaces and contain conductive material to provide electrical interconnections between components disposed on two or more substrate surfaces.

[0041] The substrate of FIG. 3 illustrates vias 306, 308, and 310. Vias 306 and 308 each provide for interconnections between components disposed on two surfaces. As shown in FIG. 3, via 306 provides for an interconnection between components disposed on surfaces 302a and 302b, while via 308 provides for an interconnection between components disposed on surfaces 302c and 302d. In